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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,470	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-14,17-22,24,25,27-29,31,32,34-36,38-40,42-46,48 and 49* is/are rejected.

7)☒ Claim(s) *4,15,16,23,26,30,33,37,41 and 47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

This Office Action is responsive to the application filed on 26 November 2003. Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 120. Claims 1-49 are presented for examination.

Claims 1-49 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 26 November 2003 was filed after the mailing date of the application on 26 November 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objection

Claim 30 is objected to because of the following informalities: in the third line of the claim, the word "in" should be replaced by "to". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 22 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As for claim 22, the Examiner does not find any disclosure in the application's specification that teaches routing the test data string from the data string manipulation circuit to the cache memory.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3, 5, 6, 8, 11, 21 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, it is unclear to the Examiner if the "data received from the second data source" refers to data used in a single comparison operation, or data used in

multiple comparison operations. The Examiner is rejecting the claim based on the former interpretation.

As for claims 3, 5, 6 and 8, is it unclear to the Examiner if the "data received from the second data source" refers to the same data received from the second data source in claim 1, or any data that is received from the second data source during any time. The examiner is rejecting claims 3 and 8 in view of the former interpretation, while rejecting claims 5 and 6 in view of the latter interpretation.

As for claim 11, it is unclear to the Examiner what "an external string execution unit" is external in reference of which structure or object of the invention.

As for claims 21 and 31, it is unclear to the Examiner if the "starting address...for said compare operation" is the address where the operation is stored in memory, or an address used by the operation. The Examiner is rejecting the claim based on the latter interpretation.

As for claim 21, the Examiner is unclear if the "cached data" in the last paragraph of the claim is referring to the "cached data stored in a cache line of the cache memory" in the second to last paragraph of the claim, or any cached data in a cache memory. The Examiner is rejecting the claim in view of the former interpretation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 7, 8, 10-14, 17-19, 21, 22, 24, 25, 27-29, 31, 32, 34-36, 38-40, 42-46 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee [5,060,143] (hereinafter "Lee"), further in view of Groves [5,222,225] (hereinafter "Groves").

As for claims 1, 3, 10, 39, 40 and 46, Lee teaches a data source (Fig 2, 110 Instruction Execution Unit) configured to hold a data value (Col 7, Lines 53-58; one of the characters in P[i]), where in the data value comprises fewer bytes than a second source of data;

a plurality of comparators (Fig 3, 140 Comparator Array) configured to compare the second source of data to the data value, each comparator having a first input coupled to said second source of data, a second input coupled to the data source and configured to receive at least a portion of the data value from the data source (Col 5, Lines 20-35; Col 8, Lines 32-44), and an output (Col 8, Lines 23-32); and

a decoder coupled to the outputs of the plurality of comparators and configured to identify a portion of the second source of data that matches at least a portion of the data value (Col 8, Lines 1-4; Col 8; Lines 44-54).

Although Lee does not particularly describe that the said second source of data is a cache line comprising a plurality of bytes of data, the prior art does discloses that the invention is implemented in a processor (Col 7, Lines 22-24) and the second source of data comes from a data base stream (Col 7, Lines 27-28). It is also obvious to one ordinarily skilled in the art at the time of the Applicant's invention that a conventional processor includes a cache memory for improved operation and access speed, and data requested by the processor are forwarded from the cache if it is found there. Furthermore, Groves discloses a string data comparison system where the source data is a cache line having a size of four bytes (Col 3, Lines 68; Col 4, Lines 1-4; Fig 2A, 20A Memory; Col 5, Lines 62-66; Fig 8). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can be used to hold the second source of data for Lee's system, in order to provide a means to store the data used for comparison operations, and to improve the operation and access speed.

It is clear that the combined cache memory described in claims 1 and 3, and the combined cache memory described in claims 39, 40 and 46 are already substantially disclosed by claim 10.

As for claims 2, 11 and 42, Lee further teaches that the data source comprises an external string execution unit (Fig 2, combination of 109 Input String Buffer, 120 Algorithm Engine, 110 Instruction Execution Unit, 112 Output Control Unit, and 114 Output Queue).

As for claim 5, Lee further teaches the data received from the second data source comprises a plurality of bytes (Col 7, Lines 53-58; P[i]).

As for claims 7 and 17, Lee further teaches, in further view of Groves, the number of the plurality of comparators is equal to the number of the bytes in the cache line (Lee: Col 4, Lines 8-11, 4 bytes and 4 comparators; Groves: Fig 2A, one cache line in Memory/Cache is 4 bytes).

As for claims 8, 18 and 48, Lee further teaches the cache line is compared to the data value in one clock cycle (Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor).

As for claims 12 and 45, Lee further teaches the decoder is configured to forward a cache line address of the matching cache line data to the string execution unit (Col 8, Lines 1-4).

As for claims 13 and 43, Lee further teaches the string execution unit comprises a bus interface unit (Fig 2, 109 Input String Buffer).

As for claims 14 and 44, Lee further teaches the string execution unit comprises an off-chip memory controller (for the string execution unit to access the data source from the cache memory for comparison as described in the above claims, there must be a memory controller comprise therein).

As for claim 19, Lee further teaches the data source comprises a processor (Col 7, Lines 42-45; instruction that contains the data value is received from a processor).

As for claims 21 and 31, Lee teaches a method for comparing data in a digital processing system with a test data string, the method comprising:

receiving an instruction (Col 7, Lines 42-45) to perform a compare operation, said instruction comprising a starting address and a test data string for said compare operation (Col 7, Lines 42-45);

routing the instruction to a data string manipulation circuit (Fig 2, combination of 109 Input String Buffer, 120 Algorithm Engine, 110 Instruction Execution Unit, 112 Output Control Unit, and 114 Output Queue);

comparing the test data string with a second source of data, wherein said test data string comprises fewer bytes than the second source of data (Col 5, Lines 20-35; Col 8, Lines 32-44); and

routing an address of the second source of data matching the test data string to the data string manipulation circuit (Col 8, Lines 1-4).

Although Lee does not particularly describe that the said second source of data is a cache line comprising a plurality of bytes of data, nor does it particularly describe routing the starting address for the compare operation from the data string manipulation circuit to a cache memory, the prior art does discloses that the invention is implemented in a processor (Col 7, Lines 22-24) and the second source of data comes from a data base stream (Col 7, Lines 27-28). It is also obvious to one ordinarily skilled in the art at the time of the Applicant's invention that a conventional processor includes a cache memory for improved operation and access speed, and data requested by the processor are forwarded from the cache if it is found there. Furthermore, Groves discloses a string data comparison system where the source data is a cache line having a size of four bytes (Col 3, Lines 68; Col 4, Lines 1-4; Fig 2A, 20A Memory; Col 5, Lines 62-66; Fig 8), and the starting address for the compare operation is routed to a cache memory (Fig 8, 132). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can be used to hold the second source of data for Lee's system, in order to provide a means to store the data used for comparison operations, and to improve the operation and access speed.

It is clear that the method of claim 31 is already substantially disclosed by claim 21.

As for claims 24 and 34, Lee further teaches the data string manipulation circuit comprises a bus interface unit (Fig 2, 109 Input String Buffer).

As for claims 25 and 35, Lee further teaches the string execution unit comprises a memory controller (for the string execution unit to access the data source from the cache memory for comparison as described in the above claims, there must be a memory controller comprise therein).

As for claims 27 and 36, Lee further teaches said act of comparing is performed by a plurality of comparators (Col 5, Lines 20-35; Col 8, Lines 32-44; Fig 3, 140 Comparator Array).

As for claim 28, Lee further teaches, in further view of Groves, the number of comparators is equal to the number of the bytes in the cache line (Lee: Col 4, Lines 8-11, 4 bytes and 4 comparators; Groves: Fig 2A, one cache line in Memory/Cache is 4 bytes).

As for claim 29, Lee further teaches said act of comparing is performed in one clock cycle (Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor).

As for claim 38, Lee further teaches said act of routing an address of cached data matching the test data is performed by a decoder (Col 8, Lines 1-4).

Claims 9, 20 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, further in view of Groves and Papworth et al. [5,404,473] (hereinafter "Papworth").

As for claims 9, 20 and 49, Lee already substantially discloses the claims in further view of Groves, but does not particularly disclose that the cache data memory comprises a Level 1 cache. However, Papworth discloses a processing system that handles string operations which comprises a Level 1 cache, in order to improve processing speed (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Lee's cache data memory in further view of Groves, can incorporate a Level 1 cache in order to improve processing speed.

Allowable Subject Matter

Claims 4, 15, 16, 23, 26, 30, 33, 37, 41 and 47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claims and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

23 November 2005

KEVIN VERBRUGGE
PRIMARY EXAMINER